~~Claims~~
WHAT IS CLAIMED

1. An integrated circuit in which at least one additional supplementary module of the same type is assigned to an individual module or a plurality of ordered modules forming cells, each with at least one input and one output, characterized in that the cells are bus systems, arithmetic and logic units and/or in particular configurable logic cells, and a first switching element is connected upstream from the input of the module and is designed to switch the input to either the module or its following module, and another switching element is connected downstream from the output and is designed to receive the output from either the module or its following module, so that in the case of an error in one of the modules, in particular an error that can be detected by a self-test, the defective module and/or function cell can be replaced by its following module by switching the switching elements, with the last module being replaced by the supplementary module.

2. The integrated circuit according to the preceding claim, characterized in that a control is provided which is designed either to switch all the switching elements in the same way or to provide two groups of switching elements, where the switching elements within one group are switched in the same way, but the two groups are switched differently to exclude a defective module from the switching elements.

3. The integrated circuit according to the preceding claim, characterized in that the control is designed to decode a binary value in such a way as to yield the first or second group circuit.

4. The integrated circuit according to one of Claims 2 or 3, characterized in that the control includes a decoder which encodes a binary value to define the switching element grouping and circuit.

5. The integrated circuit according to the preceding claim, characterized in that a counter is provided to generate the binary value.

6. The integrated circuit according to one of the preceding claims,
characterized in that a look-up table means is provided to generate the binary value.

7. The integrated circuit according to one of the preceding claims,
characterized in that a memory is provided to store a binary value indicating the defective module or all defective modules.

8. The integrated circuit according to the preceding claim, characterized in that the memory is independent of the system start.

9. A method of testing integrated circuits having cells, characterized in that the cell function of the integrated circuit is tested by executing with the cells a test program in which test vectors are calculated, where a comparison between the test result and a setpoint result is performed with at least one of the cells, and an error is indicated when the comparison indicates a deviation between the setpoint result and the test result so that in response to an error, a module having the cell found to be defective can be replaced.

10. The method according to the preceding claim,
characterized in that a cell array is tested by exchanging and/or mirroring a test algorithm which includes a plurality of calculations at least once within the array.

11. The method according to one of the preceding method claims,
characterized in that the test data required for executing the

test program is called up from an integrated memory in the integrated circuit.

12. The method according to one of the preceding method claims,
characterized in that the test method is carried out at a system start.

13. The method according to one of the preceding method claims,
characterized in that the test method is carried out as a self-test method of application programs running during waiting cycles (IDLE cycles).

14. The method according to one of the preceding method claims,
characterized in that the self-test is called up from or integrated into an application program.

15. The method according to one of the preceding method claims,
characterized in that data in arithmetic and logic units is saved in a chip-internal memory before the test algorithm is run and is loaded back into the memory after the test has run.

16. The method according to one of the preceding method claims, characterized in that registers in arithmetic and logic units are shut down before the test algorithm is run and test registers are used for the test, with the registers being connected again after the test has run.

17. The method according to one of the preceding method claims,
characterized in that in the integrated circuit at least one additional supplementary module of the same type is assigned to a number of ordered modules forming cells, each with at least one input and one output, with a first switching element

being connected upstream from the inputs of the module and being designed to switch the input to either the module or its following module; another switching element being connected downstream from the output and being designed to receive the output from either the module or its following module, with the method providing that in the case of a detected error in one of the modules, the defective module is replaced by its following module by switching the switching elements until the last module is replaced by the supplementary module.